REMARKS

The specification has been amended to correct minor obvious errors. A marked up version of the amended paragraphs of the specification is attached hereto pursuant to 37 C.F.R. § 1.121(b)(iii). Claims 1, 12 and 13 have been amended for clarity. A marked up version of the amended claims is also attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). New claims 14-24 have been added. Claims 2-11 remain unchanged. Thus, claims 1-24 are presently pending in this application for consideration.

The amendments to the present application are made to place the application in better form and to place the application in condition for allowance. No new matter has been added. Entry and consideration of these amendments prior to the first Office Action are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at Los Angeles, California, telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: July 25, 2002

By: _____

Anthony J. Orler
Registration No. 41,232
Attorney for Applicant(s)

Biltmore Tower, Suite 1900
500 South Grand Avenue
Los Angeles, California 90071
Phone: 213 337-6700
Fax: 213 337-6701

Version with markings to show changes made:

IN THE SPECIFICATION:

Please amend the specification as indicated below:

Please amend the paragraph on page 1, starting at line 20 and ending at line 21 as follows:

The present invention [may provide] provides a semiconductor device that can reduce its cell area.

Please amend the paragraph on page 1, starting at line 22 and ending at line 24 as follows:

The present invention [may] also [provide] provides a memory system and an electronic apparatus that includes a semiconductor device in accordance with the present invention.

Please amend the paragraphs on page 1, starting at line 27 and ending at page 3, line 17 as follows:

According to one aspect of the present invention, there is provided a semiconductor device [provided with a memory cell including a first load transistor, a second load transistor, a first driver transistor, a second driver transistor, a first transfer transistor, and a second transfer transistor, the semiconductor device comprising:] including a first conduction type well region[;] and a second conduction type well region[;].

The semiconductor device also includes a first gate-gate electrode layer including a gate electrode of [the] a first load transistor and a gate electrode of the first driver transistor[;] and a second gate-gate electrode layer including a gate electrode of [the] a second load transistor and a gate

electrode of the second driver transistor[;]. The semiconductor device further includes a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of [the] a first driver transistor[;] and a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of [the] a second driver transistor[;]. The semiconductor device also includes a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer[;] and a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer[,].

The [wherein the] first load transistor and the second load transistor are provided in the first conduction type well region [, wherein the] and first driver transistor and the second driver transistor are provided in the second conduction type well region[,]. The [wherein the] second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer[,]. The [wherein the] upper layer is located in a layer over the lower layer[,] and [wherein] the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

Please delete the paragraph starting at page 3, line 18 through the paragraph ending on page 6, line 20.

[Here, the "wiring layer" means a conductive layer disposed on a field or an interlayer dielectric layer.

In accordance with the present invention, the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, the pattern density of each wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area can be made smaller, compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

In this aspect, as described below, when the upper layer is provided above the second conduction type well region, a main word line can be readily provided above the first conduction type well region. Also, when the upper layer is provided above the first conduction type well region, a main word line can be readily provided above the second conduction type well region.

Concretely, the semiconductor device of this aspect may have one of the following features (1) and (2).

(1) The upper layer may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

In this feature, the main word line may be provided in the same layer as the upper layer, and may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

(2) The upper layer may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

In this feature, the main word line may be provided in the same layer as the upper layer, and may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

Further, the semiconductor device in accordance with this aspect may have one of the following features (3) to (8).

(3) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section,

the lower layer may be electrically connected to the second gate-gate electrode layer through a contact section, and

the upper layer may be electrically connected to the first drain-drain wiring layer and the lower layer through contact sections, respectively.

(4) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be provided in the same layer, and

the first drain-gate wiring layer may be provided over a border between the first conduction type well region and the second conduction type well region.

(5) The first drain-gate wiring layer and the upper layer may be provided in a manner not to overlap one another as viewed from a vertical direction.

(6) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first conductive layer,

the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and

the upper layer may be located in a third conductive layer.

(7) A second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As a result of the second conductive layer being a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniature processing can be readily performed. Accordingly, the cell area can be reduced.

(8) A second conductive layer may have a thickness of 100 to 200nm.

2. Memory System

A memory system in accordance with another aspect of the present invention is provided with the above described semiconductor device.

3. Electronic Apparatus

An electronic apparatus in accordance with further aspect of the present invention is provided with the above described semiconductor device.]

Please insert the following paragraphs starting at page 9, line 15.

<u>According to one aspect of the present invention, there is provided a semiconductor device including a first conduction type well region and a second conduction type well region.</u>

The semiconductor device also includes a first gate-gate electrode layer including a gate electrode of a first load transistor and a gate electrode of the first driver transistor and a second gate-gate electrode layer including a gate electrode of a second load transistor and a gate electrode of the second driver transistor. The semiconductor device further includes a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of a first driver transistor and a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of a second driver transistor. The semiconductor device also includes a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer and a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer.

The first load transistor and the second load transistor are provided in the first conduction type well region and first driver transistor and the second driver transistor are provided in the second conduction type well region. The second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer. The upper layer is located in a layer over the lower layer and the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

Here, the "wiring layer" means a conductive layer disposed on a field or an interlayer dielectric layer.

In accordance with the present invention, the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, the pattern density of each wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area can be made smaller, compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

In this aspect, as described below, when the upper layer is provided above the second conduction type well region, a main word line can be readily provided above the first conduction type well region. Also, when the upper layer is provided above the first conduction type well region, a main word line can be readily provided above the second conduction type well region.

Accordingly, the semiconductor device of this aspect may have one of the following arrangements:

(1) The upper layer may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

With this arrangement, the main word line may be provided in the same layer as the upper layer, and may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

(2) The upper layer may be provided above the first conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

With this arrangement, the main word line may be provided in the same layer as the upper layer, and may be provided above the second conduction type well region without exceeding a border between the first conduction type well region and the second conduction type well region.

Further, the semiconductor device in accordance with this aspect may include one of the following arrangements:

(3) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, the lower layer may be electrically connected to the second gate-gate electrode layer through a contact section, and the upper layer may be electrically connected to the first drain-drain wiring layer and the lower layer through contact sections, respectively.

(4) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be provided in the same layer, and the first drain-gate wiring layer may be provided over a border between the first conduction type well region and the second conduction type well region.

(5) The first drain-gate wiring layer and the upper layer may be provided in a manner not to overlap one another as viewed from a vertical direction.

(6) The first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in a first

conductive layer, the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in a second conductive layer, and the upper layer may be located in a third conductive layer.

(7) A second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As a result of the second conductive layer being a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniature processing can be readily performed. Accordingly, the cell area can be reduced.

(8) A second conductive layer may have a thickness of 100 to 200nm.

2. Memory System

A memory system in accordance with another aspect of the present invention is provided with the above described semiconductor device.

3. Electronic Apparatus

An electronic apparatus in accordance with further aspect of the present invention is provided with the above described semiconductor device.

IN THE ABSTRACT:

Please amend the original Abstract of the Disclosure as indicated below.

A semiconductor device is provided with [an SRAM] a memory cell. The semiconductor device includes a first gate-gate electrode layer, a second gate-gate electrode layer, a first drain-drain wiring layer, a second drain-drain wiring layer, a first drain-gate wiring layer and a second drain-gate

wiring layer. The first drain-gate wiring layer and an upper layer and a lower layer of the second drain-gate wiring layer are located in different layers, respectively. [The upper layer is provided above either an n-type well region or a p-type well region.]

IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Once Amended) A semiconductor device [provided with a memory cell including a first load transistor, a second load transistor, a first driver transistor, a second driver transistor, a first transfer transistor, and a second transfer transistor, the semiconductor device] comprising:

a first conduction type well region;

a second conduction type well region;

a first gate-gate electrode layer including a gate electrode of [the] a first load transistor and a gate electrode of [the] a first driver transistor;

a second gate-gate electrode layer including a gate electrode of [the] a second load transistor and a gate electrode of [the] a second driver transistor;

a first drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer that forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer that forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer; and

a second drain-gate wiring layer that forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer,

wherein the first load transistor and the second load transistor are provided in the first conduction type well region,

wherein the first driver transistor and the second driver transistor are provided in the second conduction type well region,

wherein the second drain-gate wiring layer is located in a layer over the first drain-gate wiring layer, and has an upper layer of the second drain-gate wiring layer and a lower layer of the second drain-gate wiring layer,

wherein the upper layer is located in a layer over the lower layer, and

wherein the upper layer is provided above one of the first conduction type well region and the second conduction type well region.

12. (Once Amended) A memory system provided with the semiconductor device according to [any one of claims] claim 1 [to 11].

13. (Once Amended) An electronic apparatus provided with the semiconductor device according to [any one of claims] claim 1 [to 11].

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ABSTRACT OF THE DISCLOSURE

A semiconductor device is provided with a memory cell. The semiconductor device includes a first gate-gate electrode layer, a second gate-gate electrode layer, a first drain-drain wiring layer, a second drain-drain wiring layer, a first drain-gate wiring layer and a second drain-gate wiring layer. The first drain-gate wiring layer and an upper layer and a lower layer of the second drain-gate wiring layer are located in different layers, respectively.